# Part B System Configuration

This part of user's manual is specifically written to help the user configure the System Board. The user can optimize the system performance by changing the default configuration of the system board.

## Features of the PCI/VL Version System Board

- SupportIntel<sup>™</sup> 486SX/DX/DX2, 486SLE, Pentium<sup>™</sup> OverDrive<sup>™</sup> Processor, Intel DX4<sup>™</sup>, P24D (Dark Green support)
- $\bullet \ \, Support Cyrix^{TM} \, 486S/S2, Cyrix \, 486DX/DX2 (light Green \, support) \\$
- Support AMD™ 486DX, AMD 486DXL (light Green support)
- Support CPU speed running at 25/33/40/50/66 Mhz
- Support 256K, 1M, 4M, 16M 30 PIN DRAM SIMM
- Support 256K, 512K, 1M, 2M, 4M, 8M, 16M 72 PIN DRAM SIMM
- Support 128/256 K Write-through / Write-back secondary Cache.
   Write-back CPU internal Cache for Cyrix.
- Support System Memory Management (SMM) and full SMI Interface support for Intel SL-Enhanced CPU (S-series)
- Two 16-bit ISA BUS expansion slots.
- Three 32-bit VL BUS/ISA BUS shared expansion slots.
- Three 32-bit PCI BUS expansion slots.
- AMI™ WinBIOS™ support system BIOS and PCI BIOS (for VL & PCI model), System and Video BIOS Shadowing, Video BIOS Cacheable. Support Plug and Play on PCI card.

## Features of VL Version System Board

- Support Intel<sup>TM</sup> 486SX/DX/DX2, 486SLE, P24T, DX4, P24D (Dark Green support)
- Support Cyrix<sup>™</sup> 486S/S2, Cyrix 486DX/DX2 (light Green support)
- Support AMD™ 486DX, AMD 486DXL (light Green support)
- Support CPU speed running at 25/33/40/50/66 Mhz
- Support 256K, 1M, 4M, 16M 30 PIN DRAM SIMM
- Support 256K, 512K, 1M, 2M, 4M, 8M, 16M 72 PIN DRAM
- Support 128/256 K Write-through / Write-back secondary Cache.
   Write-back CPU internal Cache for Cyrix.
- Support System Memory Management (SMM) and full SMI Interface support for Intel SL-Enhanced CPU (S-series)
- Two 16 bit ISA BUS expansion slots.
- Three 32 bit VL BUS/ISA BUS shared expansion slots.
- ◆ AMI<sup>™</sup> WINBIOS support system BIOS and PCI BIOS (for VL & PCI model), System and Video BIOS Shadowing, Video BIOS Cacheable. Support Plug and Play on PCI card.



There is a total of 6 SIMM sockets on the system board, they are labeled as Bank 0, SIMM 1, SIMM 2 on the system board. The system board will support 256K X 9 SIMM, 1M X 9 SIMM, 4M X 9 SIMM, 16M X 9 SIMM for 30 PIN Module, and support 256K X 36 SIMM, 512K X 36 SIMM, 1M X 36 SIMM, 2M X 36 SIMM, 4M X 36 SIMM, 8M X 36 SIMM, 16M X 36 SIMM for 72 PIN Module.

DRAM speed should be 70 ns (or faster) for 25 to 66 Mhz. Please reference to table below for DRAM combination and configuration.

DRAM Configuration Table (30 pin SIMM & 72 pin SIMM mixed)

Bank 0 (30 pin SIMM)	SIM1 (72 pin SIMM)	SIM2 (72 pin SIMM)	Total DRAM Size
256K	256K	Х	2MB
1 <b>M</b>	X	X	4MB
256K	256K	512 <b>K</b> *	4MB
256K	1 <b>M</b>	X	5MB
256K	256K	1 <b>M</b>	6МВ
1 <b>M</b>	1 <b>M</b>	x	8MB
1M	X	1 <b>M</b>	8MB
256K	256K	2M*	10MB
1 <b>M</b>	X	2M*	12MB
4M	X	X	16MB
1 <b>M</b>	1M	2M*	16MB
256K	4M	X	17MB
1 <b>M</b>	4M	X	20MB
1 <b>M</b>	X	4M	20MB
4M	4M	<b>X</b> .	32MB
4M	X	4M	32MB
16MB	X	X	64MB
4M	4M	8M*	64MB
16M	16M	Х	128MB
16M	X	16M	128MB

Remark: X - Not install

\* - Double density SIMM

### DRAM Configuration Table for (72 pin SIMM only)

Bank 0	SIM1	CVI 50	
1		SIM2	Total DRAM
(30 pin SIMM)	(72 pin SIMM)	(72 pin SIMM)	Size
x	512K*	х	2MB
X	1M	x	4MB
X	512K*	512K*	4MB
X	512 <b>K</b> *	1 <b>M</b>	6МВ
X	2M*	X	8MB
X	1M	1M	8MB
X	512 <b>K*</b>	2M*	10MB
X	1 <b>M</b>	2M*	12MB
Х	4M=	<b>X</b>	16MB
X	2M*	2M*	16MB →
X	1 <b>M</b>	4M	20MB
X	8 <b>M</b> *	X	32MB
X	4M	4M	32MB
X	16M	X	64MB
X	8M*	8M*	64MB
X	32 <b>M</b> *	X	128MB
Х	16M	16M	128M

Remark: X - Not install

\* - Double density SIMM

## **System Board Configuration**

Under some circumstances you may want to change the default configuration of the system board. These changes are made through adapting jumper settings on the system board. The following text will describle the function of jumpers and connectors and their corresponding location on the System Board can be found at the end of this chapter.

## **Jumper Functions**

### 128K Cache External Cache Size

<b>JP20</b>	U24 installed with 8Kx-15ns SRAM U25, U28, U33, U39 installed with 32Kx8-20ns SRAM
JP22	
<b>JP24</b> ⊠ ⊠  1 2	

### 256K Cache External Cache Size

JP20	U24 installed with 32Kx8-15ns SRAM U25,
1 2 3	U26, U28, U29, U33, U34, U39, U40 installed with 32Kx8-20ns SRAM
JP22, JP24 □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	

#### JP30, JP31 CPU Clock Selection

	25MHz	33MHz	40MHz	50MHz
ЈР30	1 2	1 2	1 2	1 2
JP31	1 2	1 2	1 2	1 2

### JP45 SIMM Module Selection

1 2 3	Only 72 Pin SIMM Installed, 30 Pin SIMM not Installed
* 🛛 🗷 🗷	Others

### JP39 UNIX Jumper Select

* 🗵 🗵	Normal
1 2 3	UNIX

### JP2 CMOS Data Discharge Jumper

1 2 3	Discharge
* × × × × × × × × × × × × × × × × × × ×	Normal

#### JP18 VL Bus Speed

* 🗆	CPU Speed ≤ 33MHz	
1 2	CPU Speed > 33MHz	

\* = Factory Default Value

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### JP19 VL Bus Wait State

1 2	Zero Wait State	
* XX	One Wait State	

### JP29 Local Bus Signal Adjust

* 🗵 🗵	For CPU Speed 33MHz
1 2 3	For CPU Speed 40/50MHz

\* = Factory Default Value

## **CPU Type Select Jumpers**

### INTEL 486SX CPU

<b>JP6</b>	<b>JP7</b>	JP8  □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	<b>JP10</b> <ul> <li>□ □ □</li> <li>□ □ □</li> <li>□ □ □</li> </ul>	<b>JP11</b>
JP12 ⊠⊠⊠ 1 2 3	JP13	JP14  □□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□	JP15  □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP16 1 2 3   X X X X X X X X X X X X X X X X X X X
JP17	JP21	<b>JP36</b> □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP37  □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	<b>JP38</b>

#### INTEL 486DX CPU

<b>JP6</b>	JP7	JP8	JP10  ⊠⊠⊠  1 2 3	<b>JP11</b> <a>⊠</a> <a>1 2</a>
<b>JP12</b>	JP13	<b>JP14</b>	JP15	JP16  1 2 3  □ □ □ □  4 5 6
JP17	JP21	<b>JP36</b> □ X X 1 2	JP37	<b>JP38</b>

## INTEL DX4 CPU (Internal CLK x 3)

<b>JP6</b> ⊠⊠⊠ 1 2 3	JP7 ⊠⊠⊠	<b>JP8</b> □ × 1 2	<b>JP10</b> ⊠⊠⊠ 1 2 3	JP11 ⊠ ⊠ 1 2
<b>JP12</b>	JP13	JP14 ⊠⊠⊠	JP15	JP16 1 2 3 □ □ □ □ □ □ □ □ 4 5 6
JP17	JP21	<b>JP36 X</b> 1 2	JP37	<b>JP38</b>

### INTEL 486DX4 CPU (Internal CLK x 2.5)

JP6	<b>JP7</b>	<b>JP8</b>	<b>JP10</b> <a>⊗ ⊗ ⊗</a> <a>1 2 3</a>	<b>JP11</b> (⊠ ⊠  1 2
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JP17	<b>JP21</b> □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	<b>JP36</b>	<b>JP37 ⊠</b> 1 2	<b>JP38</b>

### INTEL DX4 CPU (Internal CLK x 2)

JP6	<b>JP7</b> [□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□	JP8	JP10  ⊠ ⊠ ⊠  1 2 3	<b>JP11</b>
JP12 □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP13	JP14 □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP15 	JP16 1 2 3 □ □ □ □ □ 4 5 6
JP17	JP21	JP36	<b>JP37</b>	<b>JP38</b>

### INTEL P24D CPU

JP6 图图图	JP7 (⊠⊠ 1 2 3	JP8 [图图]	<b>JP10</b> (本 <del>図 図</del> )	JP11
JP12 (⊠ ⊠ ⊠ 1 2 3	<b>JP13</b> <a>□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □</a>	JP14 [XXX] 1 2 3	JP15	JP16 1 2 3  □ □ □ □ □ 4 5 6
JP17 □□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□	JP21	<b>JP36</b> □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP37  ⊠⊠  1 2	JP38

## INTEL Pentium OverDrive Processor CPU

JP6 ⊠⊠⊠ 1 2 3	JP7  □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP8	JP10  ⊠ ⊠ ⊠  1 2 3	<b>JP11</b> <a>□ □</a> <a>□</a> <a< th=""></a<>
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#### AMD 486DX CPU

JP6  ⊠ ⊠ ⊠  1 2 3	<b>JP7</b> □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP8	JP10 ⊠⊠⊠ 1 2 3	<b>JP11</b>
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### CYRIX 486SX CPU (1 x clk)

JP6	JP7 ⋈ ⋈ ⋈ 1 2 3	JP8	JP10 □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	<b>JP11</b> <a>⊠ ⊠</a> <a>1 2</a>
JP12 ⊠⊠⊠ 1 2 3	<b>JP13</b> ⊠⊠  1 2	<b>JP14</b> [XX   XX   XX   XX   XX   XX   XX   XX	JP15  ⊠ ⊠ ⊠ ⊠  1 2 3 4	JP16 1 2 3 XXX XXX 4 5 6
JP17 ⊠⊠ 1 2	<b>JP21</b> ⊠⊠  1 2	<b>JP36</b>	<b>JP37</b>	<b>JP38</b> ⊠⊠  1 2

### CYRIX 486SX CPU (2 x clk)

JP6  [X X X 3	<b>JP7</b> ⊠⊠⊠  1 2 3	JP8	<b>JP10</b>	<b>JP11</b>
JP12	<b>JP13</b> ဩ⊠  1 2	JP14	JP15    □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	JP16  1 2 3
<b>JP17</b>	<b>JP21</b> <a>□ □ □</a> <a>□ □</a> <a>□</a> <a>□&lt;</a>	<b>JP36</b>	<b>JP37</b>	<b>JP38</b> ☑ ☑  1 2

## CYRIX 486DX CPU (1 x clk)

<b>JP6</b>	<b>JP7</b> □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	<b>JP8</b> <a>≅ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥ ≥</a>	JP10  ⊠⊠⊠  1 2 3	<b>JP11</b> ⊠⊠  1 2
JP12 ⊠⊠⊠ 1 2 3	<b>JP13</b> <a>⊠</a> <a>1</a> <a>2</a>	JP14   X	JP15	JP16  1 2 3    X X X     X X X     4 5 6
<b>JP17</b>	<b>JP21</b> ⊠ ⊠  1 2	<b>JP36</b>	<b>JP37</b>	<b>JP38</b> ဩ⊠  1 2

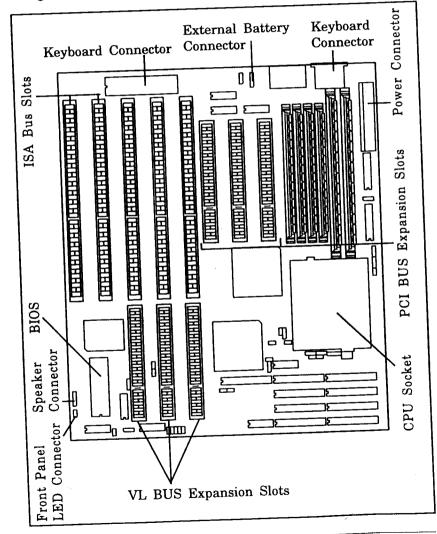
### CYRIX 486DX CPU (2 x clk)

<b>JP6</b> ⊠ <b>⊠ ⊠</b> 1 2 3	JP7	JP8	<b>JP10</b> <a>⊗ ⊗ ⋈</a> <a>1 2 3</a>	JP11 ☑⊠ 1 2
JP12 ⊠⊠⊠ 1 2 3	<b>JP13</b> ⋈ ⋈ 1 2	JP14   ⊠ ⊠ ⊠ 1 2 3	JP15	JP16 1 2 3  □ □ □ □ 4 5 6
JP17 ☑ ☑ ☑ 1 2	JP21  ⊠ ⊠  1 2	<b>JP36</b>	<b>JP37</b>	<b>JP38</b> <a>⊠ ⊠</a> <a>1 2</a>

## System Board Layout

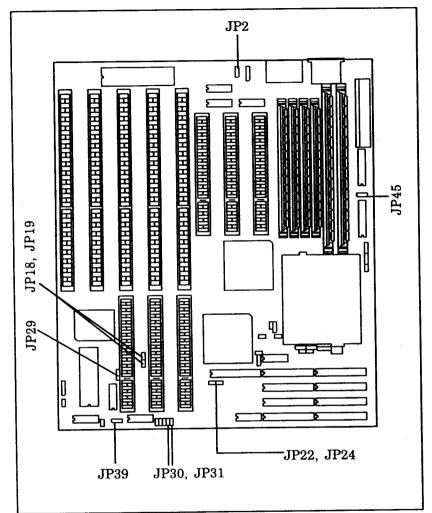
The following diagrams show the relative positions of the jumpers, connectors, major components and memory banks on the system board.

## Major Component Locations (PCI/VLVer.)

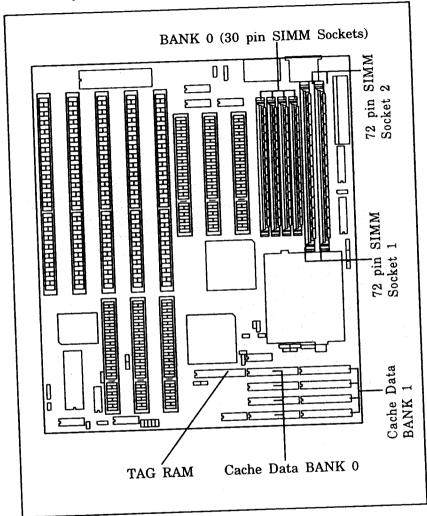


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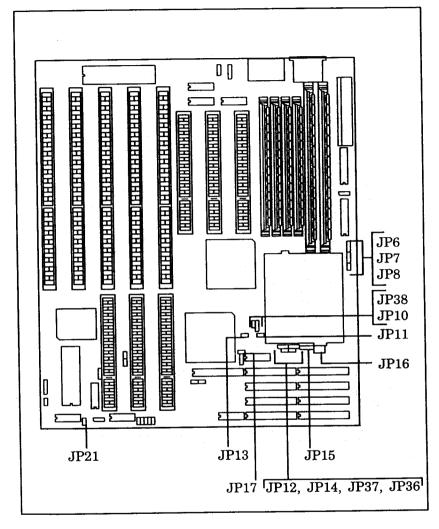
## Jumper Locations (PCI/VL Ver.)



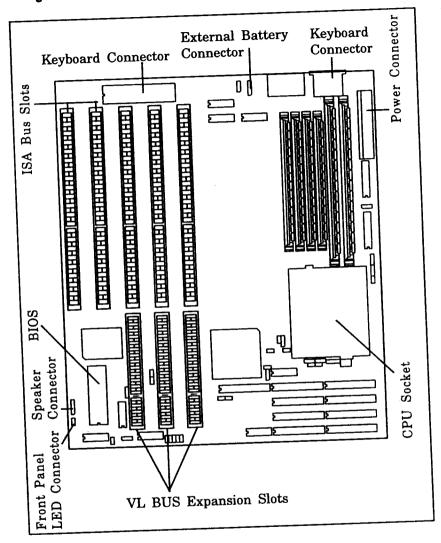
## Memory Banks (PCI/VL Ver.)



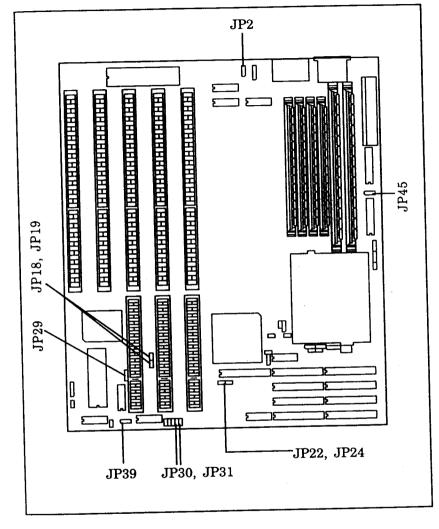
## CPU Type Select Jumpers (PCI/VL Ver.)



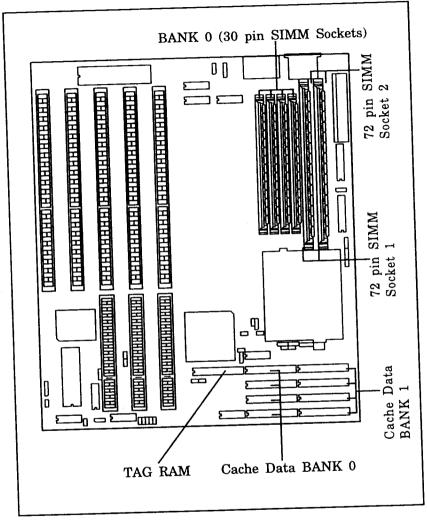
## Major Component Locations (VL Ver.)



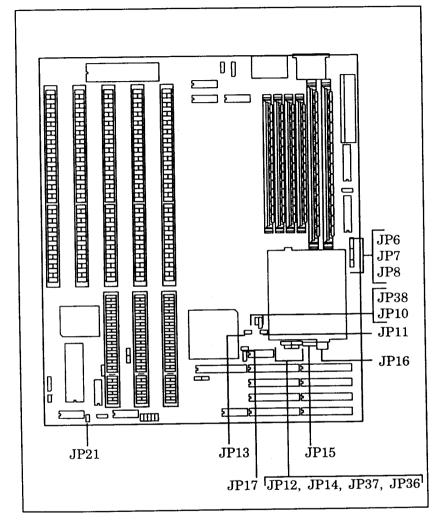
## Jumper Locations (VL Ver.)



## Memory Banks (VL Ver.)



## CPU Type Select Jumpers (VL Ver.)



### Chapter 2 WinBIOS Power-On Self Test

WinBIOS provides all IBM standard Power-On Self Test (POST) routines as well as enhanced WinBIOS POST routines. WinBIOS POST supports CPU internal diagnostics.

#### **POST Phases**

Every time the system is powered on, WinBIOS executes two types of POST routines:

System Test and Initialization (tests and initializes WinBIOS for normal operations) and

System Configuration Verification (compares defined configuration with hardware actually installed).

#### **BIOS Error Reporting**

BIOS errors are reported in one of two ways:

If the error occurs before the display device is initialized,	a series of beeps sound. Beep codes indicate that a fatal error has occurred. WinBIOS Beep Codes are described on the next page.
the error occurs after the display device is	the error message is displayed. A prompt to press <f1> can also appear with displayed error messages.</f1>

## Part C BIOS Setup

### Chapter 1 Introduction

The American Megatrends<sup>TM</sup> WinBIOS<sup>TM</sup> installed in your system is a collection of device drivers, initialization routines, system data and other code that controls the interface between the operating system software and the system hardware such as your processor and peripherals connected. The following features are included:

#### POST

Upon powering up, WinBIOS performs a series of device initialization and diagnostic tests known as the power on self test (POST). POST can generate error messages and keep codes to indicate a system problem. If an error occurs during POST before WinBIOS has initialized and configured the display monitor, beeps are sounded to indicate a system problem.

### WinBIOS Setup

WinBIOS has a system configuration utility with an easy-to-use graphical user interface, WinBIOS Setup. It is there for you to change the system configuration whenever you add new peripherals, or to fine tune the system performance. WinBIOS Setup is explained in this section.

## Chapter 2 WinBIOS Power-On Self Test

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the error occurs after the display device is	the error message is displayed. A prompt to press <f1> can also appear with displayed error messages.</f1>

### **Beep Codes**

Fatal errors, which halt the boot process, are communicated through a series of audible beeps. If WinBIOS POST can initialize the system video display, it displays the error message. Displayed error messages, in most cases, allow the system to continue to boot.

#### WinBIOS Beep Codes

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry is faulty.
2	Parity Error	Parity error in the base memory (the first 64 KB block) of memory.
3	Base 64 KB Memory Failure	Memory failure in first 64 KB.
4	Timer Not Operational	A memory failure in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor error	The CPU generated an error.
6	8042 - Gate A20 Failure	Cannot switch to protected mode.
7	Processor Exception Interrupt Error	The CPU on the CPU Card generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in WinBIOS.
10	CMOS Shutdown Register Read/Write	The shutdown register for CMOS RAM has failed.
. 11	Cache memory bad — do not enable cache	The cache memory test failed. Cach memory is disabled. Do not press <ctrl> <alt> <shift> &lt;+&gt; to enable cache memory.</shift></alt></ctrl>

## **Troubleshooting System Problems**

What to Do If the Computer Beeps

Here is what you need to do if your computer has a WinBIOS and it starts beeping:

If the system beeps	then
1, 2, or 3 times	reseat the memory SIMMs or DIPs. If the system still beeps, replace the memory.
6 times	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
11 times	reseat the cache memory on the motherboard. If it still beeps, replace the cache memory.
4, 5, 7, or 10 times	the motherboard must be replaced.

### WinBIOS Displayed Error Messages

If an error occurs after the system display has been initialized, the error messages are displayed as follows:

ERROR Message Line 1 ERROR Message Line 2 Press <F1> to continue

and the system halts. The system does not halt if Wait for  $\langle F1 \rangle$  If Any Error in Advanced Setup is Disabled.

#### RUN SETUP UTILITY.

may also appear. Press <F1> to run AMIBIOS Setup or WinBIOS Setup if this message appears.